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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/684,823      | 10/14/2003  | Ludovic Ruat         | 852663.401          | 9850             |

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SEED INTELLECTUAL PROPERTY LAW GROUP PLLC  
701 FIFTH AVENUE, SUITE 6300  
SEATTLE, WA 98104-7092

EXAMINER

NGUYEN, LINH M

ART UNIT PAPER NUMBER

2816

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/684,823

Applicant(s)

RUAT ET AL.

Examiner

Linh M. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 June 2005.  
2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-36 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-4, 6, 7, 12, 17-22, 25, 30 and 34-36 is/are rejected.  
7) ☒ Claim(s) 5, 8-11, 13-16, 23, 24, 26-29 and 31-33 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 14 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

This is a reply to the Applicant's amendment filed on 06/28/2005. By virtue of this amendment claims 1-36 are currently presented in the instant application.

#### ***Specification Objections***

1. The specification is objected to because of the following informalities:

Page 21, line 16, it is suggested to delete "T0" in front of  $(15*25 + 26)To$  in order to make the equation valid;

Page 22, line 2, it is suggested to delete "T0" in front of  $(14*25 + 2*26)To$  in order to make the equation valid;

Line 3, change "401 To" to --402To--.

Appropriate correction is required.

#### ***Claim Objections/Minor Informalities***

2. Claim 1 is objected to because of the following informalities:

Line 5, antecedent basis for "first clock signal" has already been established in line 2. It is suggested to change "a" (in front of clock signal) to --the--;

Line 7, after "pulses", it is suggested to insert --of the first clock signal -- to clarify the claimed language.

Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.  
A person shall be entitled to a patent unless –

4. Claims 1-4, 6-7, 12, 17-22, 25, 30 and 34-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Akiyama et al. (U.S. Patent No. 5,808,493).

With respect to claims 1 and 19, Akiyama et al. discloses, in Figs. 1, 2 and col. 10, lines 24-38, a programmable clock generator [Fig. 1] for delivering a first clock signal [Fout] comprising a set point M, in which M is a decimal number comprising a whole part M1 [Fig. 2, item I] and a decimal part M2 [Fig. 2, item J] and a generator configured to generate a first clock signal having a frequency that is equal to the frequency of a primary clock signal divided by the set point M, in which the period of the pulses of the first clock signal is modulated so that the duration of  $N_i$  successive pulses is substantially equal to  $M \cdot N_i$  times the period of the primary clock signal,  $N_i$  being a reference integer for the modulation of the period of the pulses of the first clock signal and wherein the primary clock signal has a determined frequency and period (*see col. 10, Eqn. 11 and lines 25-38*).

With respect to claims 2, 20 and 35, Akiyama et al. discloses, in Figs. 1, 2 and col. 10, lines 24-38, means for delivering a second clock signal the frequency of which is equal to the frequency of the first clock signal divided by an integer N (*inherently, in the case when the decimal part, J, is equal to zero*).

With respect to claims 3, 21 and 36, Akiyama et al. discloses, in Figs. 1, 2 and 12, and col. 10, lines 24-38, that  $N_i$  is equal to N.

With respect to claims 4 and 22, Akiyama et al. discloses, in Figs. 1-2, and col. 10, lines 24-38, that the decimal part M2 of the set point M is a binary coded rational number representing a fraction that can be modulated by increments equal to  $1/N_i$ .

With respect to claim 6, Akiyama et al. discloses, in Figs. 1-2, a circuit [6] receiving at its input the whole part M1 [I] of the set point and the numerator of the rational decimal part M2 [J] of the set point.

With respect to claim 7, Akiyama et al. discloses, in Figs. 1-2, and col. 10, lines 24-38 means for modulating [21] the period of the pulses of the first clock signal, arranged to deliver pulses of the first clock signal the period of which is equal to the period of the primary clock signal multiplied by a whole number the value of which is variable.

With respect to claims 12 and 30, Akiyama et al. discloses, in Figs. 1-2, and col. 10, lines 24-38, that the modulation means [21] are driven by a modulation distribution circuit arranged to distribute in a determined manner, in a group of  $N_i$  successive pulses, the pulses having their period modulated.

With respect to claim 17, Akiyama et al. discloses, in Figs. 1-2, and 12, and col. 10, lines 24-38, a universal asynchronous circuit, comprising a programmable clock generator [Fig. 1] to deliver, using a primary clock signal of determined frequency and period, a first clock signal [Fout] having a frequency that is equal to the frequency of the primary clock signal divided by a set point M, the generator comprising means for modulating a period of the pulses of the first clock signal, wherein the set point M is a decimal number comprising a whole part M1 [Fig. 2, item I] and a decimal part M2 [Fig. 2, item J], so that the duration of  $N_i$  successive pulses is substantially equal to  $M \cdot N_i$  times the period of the primary clock signal,  $N_i$  being a reference

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integer for the modulation of the period of the pulses of the first clock signal (*see col. 10, Eqn. 11 and lines 25-38*).; and an oversampling register [[Fig. 12, item 39] linked to a data receiving terminal, the register being driven by an oversampling clock signal, wherein the first clock signal delivered by the clock generator forms the oversampling clock signal.

With respect to claims 18 and 34, Akiyama et al. discloses, in Figs. 1-2, and 12, the step of using a bit clock signal to receive or send data, the frequency of the bit clock signal being equal to the frequency of the first clock signal divided by the reference integer  $N_i$  of the clock generator circuit.

With respect to claim 25, Akiyama et al. discloses, in Figs. 1-2, and 12 and col. 10, lines 24-38, that the method including the step of multiplying the period of the primary clock signal by a whole number [I] the value of which is variable to modulate the period of the pulses of the first clock signal [Fout].

#### ***Allowable Subject Matter***

5. Claims 5, 8-11, 13-16, 23-24, 26-29, and 31-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

a) A clock generator, in which the decimal part M2 is a fraction between  $-(N_i-1)/(2*N_i)$  and +0.5 or between -0.5 and  $+(N_i-1)/(2*N_i)$  by increments equal to  $1/N_i$ , as called for in claims 5 and 23;

b) The clock generator, in which the modulation means are arranged to deliver pulses of the first clock signal the period of which is modulated on two values equal to  $M1 \cdot T_o$  and  $(M1+1) \cdot T_o$ ,  $T_o$  being the period of the primary clock signal, as called for in claims 8 and 26;

c) The clock generator, in which the modulation means are arranged to deliver pulses of the first clock signal the period of which is modulated on two values equal to  $M1 \cdot T_o$  and  $(M1-1) \cdot T_o$ ,  $T_o$  being the period of the primary clock signal, as called for in claims 9 and 27;

d) The clock generator, in which the modulation means are arranged to deliver pulses of the first clock signal the period of which is modulated on three values  $(M1-1) \cdot T_o$ ,  $M1 \cdot T_o$  and  $(M1+1) \cdot T_o$ ,  $T_o$  being the period of the primary clock signal, as called for in claims 10 and 28;

e) The clock generator, in which the modulation means includes a multiplexer circuit receiving at input several division set points the value of which varies by whole increments around the whole part  $M1$  of the set point  $M$ , delivering a set point of variable value selected from the several division set points, and a divider of the frequency of the primary clock signal receiving at one input the variable value set point selected by the multiplexer circuit, as called for in claims 11 and 29;

f) The clock generator, in which the distribution circuit first modulates the period of the first and last pulses out of a group of  $N_i$  successive pulses of the first clock signal, and gives the period of the middle pulses of the group of  $N_i$  pulses a non-modulated value, as called for in claims 13 and 31;

g) The clock generator, in which when  $M2$  is higher than 0.5 the distribution circuit modulates the period of the pulses of the first clock signal by lower values by using the value

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To\*(M1+1) as a non-modulated value, To being the period of the primary clock signal, as called for in claims 14 and 32;

h) The clock generator, in which when M2 is lower than 0.5 the distribution circuit modulates the period of the pulses of the first clock signal by higher values by using the value To\*(M1) as a non-modulated value, To being the period of the primary clock signal, as called for in claims 15 and 33;

i) The clock generator, in which the distribution circuit comprises a hard-wired logic block receiving the decimal part M1 of the set point M at input and delivering to the modulation means, upon each new pulse of the first clock signal, a select signal for selecting the whole number determining the period of the pulse of the first clock signal, as called for in claim 16; and

j) A method, in which the step of coding of the rational number M2 only includes coding of the numerator of the rational number M2, the denominator of which is a predetermined number, as called for in claim 24.

### ***Remarks***

7. Applicant's remarks filed 06/28/2005 with respect to the rejection of claims 1-36 have been fully considered; however, upon further consideration, a new ground of rejection is made in view of newly discovered prior art to Akiyama et al. as set forth in the office action.

### ***Inquiry***

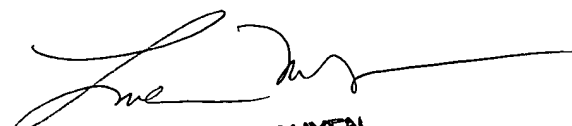
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN



LINH MY NGUYEN  
PRIMARY EXAMINER